In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended. Claims 19 and 20, indicated to be allowable, have been combined with claims 1 and 10, respectively and claims 14 - 20 have been canceled without disclaimer or prejudice to further pursuit of original claims in a continuing application.

1. (Currently Amended) A semiconductor integrated circuit, comprising:
a) a semiconductor-on-insulator (SOI) region with a buried dielectric layer;
b) a bulk semiconductor region adjacent to the SOI region;
c) a trench filled with epitaxial semiconductor material disposed between the SOI region and bulk region

wherein said epitaxial semiconductor material has a crystal orientation corresponding to crystal orientation of said SOI region adjacent said SOI region and a crystal orientation corresponding to said bulk semiconductor region adjacent said bulk semiconductor region and includes a transition of crystal orientation at approximately a center of said epitaxial semiconductor material if said crystal orientation of said SOI region and said crystal orientation of said bulk semiconductor region are different.

2. (Original) The semiconductor integrated circuit of claim 1 further comprising a buried sidewall spacer between the SOI region and bulk region, and disposed under the trench filled with epitaxial semiconductor material.

3. (Original) The semiconductor integrated circuit of claim 1 further comprising:
a) a first type doping in the bulk region;
b) a second type doping in the SOI region;
c) a butted P-N junction between the first-type doping and second type doping, wherein the butted junction is disposed in the SOI region, or in the filled trench.

4. (Original) The semiconductor integrated circuit of claim 3 wherein the first type doping extends into the SOI region.

5. (Original) The semiconductor integrated circuit of claim 3 wherein the trench filled with epitaxial semiconductor material has the first type doping.

6. (Original) The semiconductor integrated circuit of claim 3 further comprising a metal silicide layer disposed on the butted P-N junction.

7. (Original) The semiconductor integrated circuit of claim 6 wherein the metal silicide layer is disposed on a portion of the bulk region having the first type doping and on a portion of the SOI region having the second type doping.

8. (Original) The semiconductor integrated circuit of claim 1 wherein the SOI region and bulk region have different crystal orientations.

9. (Original) The semiconductor integrated circuit of claim 8 wherein the SOI region and bulk region are made of silicon, and wherein the SOI region has a {110} crystal orientation, and the bulk region has a {100} crystal orientation.

10. (Currently Amended) A semiconductor integrated circuit, comprising:
a) a semiconductor-on-insulator (SOI) region with a buried dielectric layer;
b) a bulk semiconductor region adjacent to the SOI region;
c) a P-N junction formed from a first type doping in the bulk region and a second type doping in the SOI region;
d) a metal silicide layer disposed on and electrically bridging the P-N junction

wherein epitaxial semiconductor material has a crystal orientation corresponding to crystal orientation of said SOI region adjacent said SOI region and a crystal orientation corresponding to said bulk semiconductor region adjacent said bulk semiconductor region and includes a transition of crystal orientation at approximately a center of said epitaxial semiconductor material if said crystal orientation of said SOI region and said crystal orientation of said bulk semiconductor region are different.

11. (Original) The semiconductor integrated circuit of claim 10 wherein the P-N junction is disposed in the SOI region.

12. (Original) The semiconductor integrated circuit of claim 10 wherein the P-N junction is disposed at the trench filled with epitaxial semiconductor material.

13. (Original) The semiconductor integrated circuit of claim 10 further comprising a trench filled with epitaxial semiconductor material disposed between the SOI region and bulk region;

14. - 20. (Canceled)